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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,393	02/10/2004	Hillery C. Hunter	YOR920030591US1	8889

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EXAMINER	
LE, DIEU MINH T	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,393	HUNTER ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26, 28-34* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-34 are presented for examination.

Double Patenting Rejections

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer **cannot** overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1-19 are rejected under 35 U.S.C. 101 as claiming **the same invention** as that of claims 1-20 of prior U.S. Patent No. 6,898,261. This is a double patenting rejection.

Applicant is required to cancel claims 1-19 from this application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 20-26, and 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (U.S. 6,026,354 hereafter referred to as Singh) in view of Wiedenman et al. (U.S. 7,051,131 hereafter referred to as Wiedenman).

As per claim 20:

Singh substantially teach the invention. Singh teaches:

- A method for monitoring event occurrences from a plurality of functional processor units at a centralized location via a dedicated bus coupled between said plurality of functional processor units and said centralized location [fig. 1, col. 1, lines 54-64; col. 3, lines 1-5] method comprising:

- receiving, at said centralized location, data indicative of cumulative events occurring at one of said functional processor units [col. 2, lines 17-27; col. 3, lines 6-25];

- storing said data in a first temporary memory [fig. 1, col. 1, lines 54-64; col. 3, lines 6-25];

- storing said data in a register [fig. 1, col. 2, lines 5-17; col. 4, lines 18-33].

Singh does not explicitly address:

- a tag identifier affixed to said data.

However, Singh does disclose capability of:

- A method and system for monitoring component within a computer system via dedicated bus and processor [abstract, fig. 1, col. 8, lines 20-30] comprising:

- *a connectivity among processor units, controller, memory, diagnostics components via communication bus* [figures 1, col. 2, lines 55 through col. 3, lines25];

- ***data memory reading/writing and mapping into memory space via control register, event log, and device type identification*** [col. 4, lines 18-34; col. 5, lines 1-15; and col. 8, table 4 (i.e., ***data/device index, date/time, event code and event data***].

In addition, Wiedenman explicitly teaches:

- A method and apparatus for monitoring bus activity in a multi-processor environment [abstract, fig. 1-3, col. 13, lines 65 through col. 14, line 15] comprising:

  - ***a register base control used for data configuration, monitoring events via component identifier interface*** [col. 8, lines 56 through col. 9, lines 12 and col. 14, lines 27-42].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Singh's ***data memory reading/writing and mapping into memory space via control register, event log, and device type identification*** as being the tag identifier affixed to data as claimed by Applicant. This is because Singh explicitly performed data configuring, data transmission, data/event monitoring in supporting the data processing and/or configuring including failure detection and recovery via data/error monitoring, detecting, and correcting processes. By utilizing these capabilities, the data between the data storage device and information data communication system (i.e., host/processor unit/servers/gateways/switches environment) can be directed or redirected promptly and functioned properly via

its event monitoring operation; second, by applying the ***register base control used for data configuration, monitoring events via component identifier interface*** as taught by Wiedenman in conjunction with the method and system for monitoring component within a computer system via dedicated bus and processor as taught by Singh, the device monitoring networking system including its register based on data configuration (i.e., data identifier) can enhance its operation performance, more specifically to ensuring the data monitored and routed via dedicated bus in the storage area network area.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer system operation availability and network/system performance therein with a mechanism to enhance the data monitoring, data connectivity, data debugging, data comparison, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claim 21 and 28:

Singh further teaches:

- sending said data to a controller adapted to examine said data to determine whether said one of said plurality of

functional processor units is to be reconfigured to operate in a different manner [col. 2, lines 17-27; col. 3, lines 6-25; and col. 8, lines 52-58];

- register is logically combined with a value originating from other functional processor units [col. 4, lines 18-34; col. 5, lines 1-15].

In addition, Wiedenman explicitly teaches:

- A method and apparatus for monitoring bus activity in a multi-processor environment [abstract, fig. 1-3, col. 13, lines 65 through col. 14, line 15] comprising:

- ***a register base control used for data configuration, monitoring events via component identifier interface*** [col. 8, lines 56 through col. 9, lines 12 and col. 14, lines 27-42].

- register is logically combined with a value originating from other functional processor units [col. 14, lines 27-43].

As per claim 22:

Singh further teaches:

- receiving, at said centralized location, data indicative of cumulative events occurring at one of said functional processor units [col. 2, lines 17-27; col. 3, lines 6-25];

Singh does not explicitly address:

- data comprises one of a pattern history and a count value.

However, Singh does disclose capability of:

- A method and system for monitoring component within a computer system via dedicated bus and processor [abstract, fig. 1, col. 8, lines 20-30] comprising:

- *a connectivity among processor units, controller, memory, diagnostics components via communication bus* [figures 1, col. 2, lines 55 through col. 3, lines25];

- ***data log, event log and report*** [col. 5, lines 45 through col. 6, lines 35].

In addition, Wiedenman explicitly teaches:

- A method and apparatus for monitoring bus activity in a multi-processor environment [abstract, fig. 1-3, col. 13, lines 65 through col. 14, line 15] comprising:

- ***data history including history tracking activity, history memory, history data control register*** [abstract, col. 2, lines 45-50 and col. 14, lines 47 through col. 15, lines 12].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Singh's ***data log, event log and report*** as being the data comprises one of a pattern history and a count value as claimed by Applicant. This is because Singh explicitly performed data reporting, data/event monitoring in supporting the data processing and/or configuring within the data computer system. By utilizing these capabilities, the data resided with the data storage device can be tracked, compared, and configured within the history of data memory via its event monitoring operation in supporting the data monitoring process; second, by applying the ***data history including history tracking activity, history memory, history data control register*** as taught by Wiedenman in conjunction with the method and system for monitoring component within a computer system via dedicated bus and processor as taught by Singh, the device monitoring networking system can enhance its operation performance via dedicated bus in the storage area network area.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer system operation availability and network/system performance therein with a mechanism to enhance the data monitoring, data connectivity, data debugging, data comparison, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 23-24:

Singh further teaches:

- performing an arithmetic-logic operation on said received data prior to storing said data in said register [col. 2, lines 17-27; col. 3, lines 6-25; and col. 8, lines 52-58];
- receiving, at said controller, said data collected from said digest controller [col. 4, lines 18-34; col. 5, lines 1-15]

- comparing said collected data to a predetermined value (i.e., polling value) [col. 8, lines 35-38];

- generating an instruction message based on said comparison [col. 8, lines 38-51];

- sending said instruction message to said one of a plurality of functional processor units [col. 8, lines 59-67].

In addition, Wiedenman explicitly teaches:

- A method and apparatus for monitoring bus activity in a multi-processor environment [abstract, fig. 1-3, col. 13, lines 65 through col. 14, line 15] comprising:

- ***a register base control used for data configuration, monitoring events via component identifier interface*** [col. 8, lines 56 through col. 9, lines 12 and col. 14, lines 27-42].

- register is logically combined with a value originating from other functional processor units [col. 14, lines 27-43]

- comparing said collected data to a predetermined value [col. 16, lines 39-50];

As per claims 25-26:

Singh further teaches:

- receiving, at said centralized location, data indicative of cumulative events occurring at one of said functional processor units [col. 2, lines 17-27; col. 3, lines 6-25];

Singh does not explicitly address:

- affixed instruction tag over dedicated bus.

However, Singh does disclose capability of:

- A method and system for monitoring component within a computer system via dedicated bus and processor [abstract, fig. 1, col. 8, lines 20-30] comprising:

- *a connectivity among processor units, controller, memory, diagnostics components via communication bus* [figures 1, col. 2, lines 55 through col. 3, lines25];

- data memory reading/writing and mapping into memory space via control register, event log, and device type identification including ***instruction I/O used for control register access*** [col. 4, lines 18-34; col. 5, lines 1-15; and col. 8, table 4 (i.e., data/device index, date/time, event code and event data].

In addition, Wiedenman explicitly teaches:

- A method and apparatus for monitoring bus activity in a multi-processor environment [abstract, fig. 1-3, col. 13, lines 65 through col. 14, line 15] comprising:

- ***a register base control used for data configuration, monitoring events via component identifier interface*** [col.

8, lines 56 through col. 9, lines 12 and col. 14, lines 27-42].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Singh's data memory reading/writing and mapping into memory space via control register, event log, and device type identification including ***instruction I/O used for control register access*** as being the tag identifier affixed instruction tag over dedicated bus as claimed by Applicant. This is because Singh explicitly performed data configuring, data transmission, data/event monitoring in supporting the data processing and/or configuring including failure detection and recovery via data/error monitoring, detecting, and correcting processes; second, by applying the ***register base control used for data configuration, monitoring events via component identifier interface (i.e., instruction embedded)*** as taught by Wiedenman in conjunction with the method and system for monitoring component within a computer system via dedicated bus and processor as taught by Singh, the device monitoring networking system including its register based on data configuration (i.e., data identifier) can enhance its operation

performance for the same reasons set forth as described in claim 20, **supra.**

As per claims 29-34:

Due to the similarity of claims 29-34 to claims 20-26 and 28 except for a digest collector for centrally monitoring event occurrences at a plurality of functional processor units comprising a bus, a register file, a control circuit, a tag identifying, etc… instead of a method for monitoring event occurrences from a plurality of functional processor unit comprising a bus, a register file, a control circuit, a tag identifying, etc as described in claims 20-26 and 28; therefore, these claims are also rejected under the same rationale applied against claims 20-26 and 28. **In addition, all of the limitations have been noted in the rejection as per claims** 20-26 and 28. Such as ***a connectivity among processor units, controller, memory, diagnostics components via communication bus is illustrated by Singh as depicted in figures 1, col. 2, lines 55 through col. 3, lines25***].

Allowable Subject Matter

7. Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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12/9/06